AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An integrated circuit device having a plurality of input terminals, comprising:

a plurality of input buffers provided to the plurality of input terminals;

a plurality of serial to parallel conversion circuits for converting outputs of the input buffers from serial to parallel; and

a plurality of boundary scan registers, serially connected to constitute a shift register, for inputting and outputting scan-in data or scan-out data, the scan-in data being input to the shift register and the scan-out data being output from the shift register ~~which input selectively an output of the input buffer or an input of a test data, holds the input data, and outputs selectively the held input data or an output of the serial parallel conversion circuit~~,

wherein each of the boundary scan registers selectively input an input data including one of an output of the input buffer and the scan-in or scan-out data, holds the input data, and selectively output either the input data or an output from one of the serial to parallel conversion circuits ~~the plurality of boundary scan registers are connected serially to constitute a shift register~~.

2. (Currently Amended) The integrated circuit device according to claim 1, wherein one of the boundary scan registers comprises:

a first selector circuit for selectively inputting the output of the input buffer or the input of the ~~test data~~ scan-in data or scan-out data; and

a second selector circuit for selectively outputting the held input data or the output of the serial to parallel conversion circuit.

3. (Currently Amended) The integrated circuit device according to claim 2, wherein the serial to parallel conversion circuit has a plurality of outputs, and the second selector ~~circuits are~~ circuit is provided in correspondence to the plurality of outputs of the serial to parallel conversion circuit.

4. (Currently Amended) The integrated circuit device according to claim 1, wherein the input terminals include differential input terminal pairs for inputting differential inputs, respectively, and one of the input buffer receives the differential ~~input~~ inputs, and outputs an input of the serial to parallel conversion circuit.

5. (Currently Amended) An integrated circuit device having a plurality of output terminals, comprising:

a plurality of parallel to serial conversion circuits for converting an internal signal from parallel to serial;

a plurality of output buffers which are provided to the plurality of output terminals, and to which an output of the parallel to serial conversion circuit is supplied; and

a plurality of boundary scan registers, serially connected to constitute a shift register, for inputting and outputting scan-in data or scan-out data, the scan-in data being input to the shift register and the scan-out data being output from the shift register

~~which selectively input the internal signal or an input of a test data, hold the input data, and selectively output the held input data or an output of the output buffer~~,

wherein each of the boundary scan registers selectively input an input data including one of an output of the input buffer and the scan-in or scan-out data, holds the input data, and selectively output either the input data or an output from one of the serial to parallel conversion circuits ~~the plurality of boundary scan registers are serially connected to constitute a shift register~~.

6. (Currently Amended) The integrated circuit device according to claim 5, wherein one of the boundary scan registers comprises:

a first selector circuit for selectively inputting the internal signal or the input of the ~~test data~~ scan-in data or scan-out data; and

a second selector circuit for selectively outputting the held input data or the output of the output buffer.

7. (Original) The integrated circuit device according to claim 6, wherein the output buffer outputs a differential output, and the second selector circuit selectively outputs a complementary signal of the held input data or the differential output of the output buffer.

8. (Currently Amended) The integrated circuit device according to claim 6, wherein a plurality of the internal signals are input into the parallel to serial conversion

circuit, and an AND signal, an OR signal, or an exclusive OR signal of the plurality of internal signals are input to the first selector circuit as the internal signal.

9. (Currently Amended) An integrated circuit device having a plurality of output terminals, comprising:

a plurality of parallel to serial conversion circuits for converting an internal signal ~~for~~ from parallel to serial;

a plurality of output buffers which are provided to the plurality of output terminals, and to which an output of one of the parallel to serial conversion circuits is supplied;

a plurality of boundary scan registers, serially connected to constitute a shift register, for inputting and outputting scan-in data or scan-out data, the scan-in data being input to the shift register and the scan-out data being output from the shift register ~~which selectively input the internal signal or an input of the test data, hold the input data, and selectively output the held input data or an output of the parallel serial conversion circuit~~,

wherein each of the boundary scan registers selectively input an input data including one of an output of the input buffer and the scan-in or scan-out data, holds the input data, and selectively output either the input data or an output from one of the serial to parallel conversion circuits ~~the plurality of boundary scan registers are serially connected to constitute a shift register~~.

10. (Currently Amended) The integrated circuit device according to claim 9, wherein one of the boundary scan ~~register~~ registers comprises:

a first selector circuit for selectively inputting the internal signal or the input of the ~~test data~~ scan-in or scan-out data ; and

a second selector circuit for selectively outputting the held input data or the output of the parallel to serial conversion circuit.